



**UNITED STATES DEPARTMENT OF COMMERCE**  
**Patent and Trademark Office**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/467,992 12/20/99 FORBES

L 303.389US2

021186 MM91/1010  
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EXAMINER

LEE, E

ART UNIT

PAPER NUMBER

2815  
DATE MAILED:

10/10/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

# Office Action Summary

Application No.

09/467,992

Applicant(s)

FORBES ET AL.

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 20 December 1999.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 17-19,22,23,26,27,29 and 31-50 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 17-19,22,23,26,27,29 and 31-50 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the lateral transistor, trench capacitor, and conductorless electrical connection must be shown or the feature(s) canceled from the claim(s). FIG. 1 shows a vertical transistor, not a lateral transistor. FIG. 6 contains a lateral transistor, however, the electrical connection is not conductorless as shown by strap 630. No new matter should be entered.

### ***Specification***

2. The amendment filed 7/20/01 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: a first plate of polycrystalline material formed in the trench that is coupled to a second plate integral with the first source/drain region thereby forming a conductorless electrical connection between the trench capacitor and the transistor. See paragraph 4 below.

Applicant is required to cancel the new matter in the reply to this Office Action.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

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pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 17 thru 19, 22, 23, 26, 27, 29, 31 thru 50 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not sufficiently disclose a first plate of polycrystalline material formed in the trench that is coupled to a second plate integral with the first source/drain region thereby forming a conductorless electrical connection between the trench capacitor and the transistor. The Office does not see how either plate 110 or 120 could be construed as being coupled to each other. The second plate 120 is electrically isolated from second source/drain 110 by gate insulator 122. The first source/drain region is isolated from the second source/drain 110 (also known as the first plate) by a body region. The Office does not see how a second plate 120 could be integral with the first source/drain region 106 when they are clearly isolated from each other." The body region 108 is not conductorless and can not be construed as a "conductorless" electrical connection.

Also, the specification does not support a lateral transistor with a conductorless electrical connection included.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 17 thru 19, 22, 23, 26, 27, 29, 31 thru 50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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It is unclear whether the first plate cited on page 6, line 27 is element 110. It is also unclear what the applicant means by the word "integral." The Office has provisionally interpreted the word "integral" to mean that the first plate is the same structure as the source/drain region 110 since it is formed in a trench. However, appropriate confirmation and correction are required.

It is unclear whether the first plate of polycrystalline material and the second source/drain are the same structure. The claim, as currently written, discloses the first plate of polycrystalline material and the second source/drain as separate structures. The first plate could not be construed as the substrate 101 since the claims recite the first plate as being made of polycrystalline material in a trench.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Insofar as definite, claims 17 thru 19, 22, 23, 26, 27, 29, 31 thru 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wen '509. For example, in FIG. 3, Wen discloses a memory cell trench storage capacitor 100 comprising a polysilicon layer (second plate) 114, capacitor dielectric layer (insulator layer) 116, doped polysilicon fill (first plate) 118 and p+ doped semiconductor substrate 110.

Regarding the above claims, it is well known in the art that capacitor plates are inherently connected to source/drain regions of peripheral transistors. It is also well known that bit and word lines are coupled to source/drain regions and gates of access transistors along with a column decoder and row decoder to access the cells of an array. These positions are supported by Pfister '385, Forbes et al. '618, and Wahlstrom '452.

The basis of the combination is that Wen's trench capacitor is used in conventional memory cells, for example, like the ones shown in Pfister '385, Forbes et al. '618 and Wahlstrom '452. It would have been obvious to one of ordinary skill in the art at the time of invention to use the trench capacitor of Wen in typical memory cells like Pfister, Forbes and Wahlstrom since Wen specifically states that the trench capacitor is used for memory cells and, therefore, can provide a capacitor with increased surface area and capacitance for the memory cell (as stated in the abstract) to offset the continued miniaturization of semiconductor devices.

### ***Product-by-Process Limitations***

9. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a

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new method is not patentable as a product, whether claimed in “product by process” claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Therefore, no patentable weight will be given to claim language that does not offer any structural variation to the final product.

### ***Prior Art***

10. The prior art of made of record and not relied upon is considered pertinent to applicant's disclosure. See, for example, Koyabayashi et al. '788 B1 wherein Koyabayashi describes the substrate (source/drain) as being made of polycrystalline silicon out of one of many materials (column 2, lines 65-\*). Also, Sudharsanan et al. '708 B1 describes polycrystalline silicon as being a cheaper material than single crystalline materials (column 4, lines 37-44).

### ***Response to Arguments***

11. Applicant's arguments filed 7/20/01 have been fully considered but they are not persuasive. The Office does not see the “conductorless” electrical connection cited by the applicant. Observing FIG.1, the Office does not see how either plate 110 or 120 could be construed as being electrically connected to the source/drain regions of a transistor.

Regarding the applicant's argument that polycrystalline silicon is not a suitable material for forming the source and drain regions of a transistor, the Office concurs that for the reasons cited, polycrystalline silicon is not the best choice, however, it was well known in the art at the

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time of invention that polycrystalline silicon was a cheaper alternative in semiconductor devices.

See, for example, *Prior Art* paragraph above.

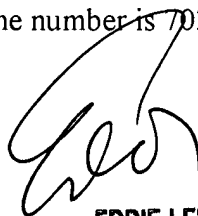
### INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee  
October 4, 2001



**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
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